IN THE CLAIMS:

Please amend the claims as set forth below:

1. (Currently Amended) A way predictor comprising:

a decoder configured to decode an indication of a first address that is to access a cache, the decoder configured to select a set responsive to the indication of the first address;

a memory coupled to the decoder, wherein the memory is configured to output a plurality of values from the set ~~a set of storage locations~~ in response to the decoder selecting the set, wherein each of the plurality of values corresponds to a different way of the cache, wherein each of the plurality of values comprises a plurality of bits associated with a corresponding cache line stored in the cache; and

a circuit coupled to receive the plurality of values and a first value corresponding to the first address, wherein the circuit is configured to generate a way prediction for the cache responsive to the plurality of values and the first value.

2. (Currently Amended) The way predictor as recited in claim 1 wherein the circuit comprises a plurality of comparators, wherein each comparator of the plurality of comparators is configured to compare a respective one of the plurality of values to the first value, and wherein the circuit is configured to generate the way prediction predicting a first way of the cache for which the corresponding value of the plurality of values matches the first value as indicated by the plurality of comparators.

3. (Original) The way predictor as recited in claim 2 wherein the circuit, if none of the plurality of values matches the first value, is configured to assert an early miss signal.

4. (Original) The way predictor as recited in claim 1 wherein each of the plurality of values comprises a portion of a tag identifying a corresponding cache line in the cache, the portion excluding at least one bit of the tag.

5. (Original) The way predictor as recited in claim 1 wherein each of the plurality of values is derived from at least a portion of the indication of the address identifying a corresponding cache line.

6. (Original) The way predictor as recited in claim 5 wherein each of the plurality of values comprises a portion of one or more address operands used to generate the address.

7. (Original) The way predictor as recited in claim 5 wherein at least one bit of one of the plurality of values is a logical combination of two or more bits of the address.

8. (Original) The way predictor as recited in claim 5 wherein at least one bit of one of the plurality of values is a logical combination of two or more bits of one or more address operands used to generate the address.

9. (Original) The way predictor as recited in claim 1 wherein the indication of the first address comprises at least a portion of the first address.

10. (Currently Amended) The way predictor as recited in claim 1 wherein the indication of the first address comprises ~~one~~ two or more address operands used to generate the first address.

11. (Original) The way predictor as recited in claim 1 wherein, if the way prediction is incorrect, the cache is configured to replace a cache line in the way indicated by the way prediction with a missing cache line corresponding to the first address.

12. (Original) The way predictor as recited in claim 11 wherein, if no way prediction is generated and a cache miss results for the first address, the cache is configured to use a

replacement algorithm to select the cache line to be replaced with the missing cache line.

13. (Currently Amended) A method comprising:

decoding an indication of a first address that is to access a cache to select a set;

outputting a plurality of values from ~~a set of storage locations~~ the set in a memory in response to the set being selected, wherein each of the plurality of values corresponds to a different way of the cache, wherein each of the plurality of values comprises a plurality of bits associated with a corresponding cache line stored in the cache; and

generating a way prediction for the cache responsive to the plurality of values and a first value corresponding to the first address.

14. (Currently Amended) The method as recited in claim 13 wherein the generating comprises comparing each of the plurality of values to the first value, and wherein the way prediction predicts a first way of the cache for which the corresponding value of the plurality of values matches the first value as indicated by the comparing.

15. (Original) The method as recited in claim 14 further comprising, if none of the plurality of values matches the first value, indicating a miss.

16. (Original) The method as recited in claim 13 wherein each of the plurality of values comprises a portion of a tag identifying a corresponding cache line in the cache, the portion excluding at least one bit of the tag.

17. (Original) The method as recited in claim 13 wherein each of the plurality of values is derived from at least a portion of the indication of the address identifying a corresponding cache line.

18. (Original) The method as recited in claim 17 wherein each of the plurality of values comprises a portion of one or more address operands used to generate the address.

19. (Original) The method as recited in claim 17 wherein a bit of each of the plurality of values is a logical combination of two or more bits of the address.

20. (Original) The method as recited in claim 17 wherein a bit of each of the plurality of values is a logical combination of two or more bits of one or more address operands used to generate the address.

21. (Original) The method as recited in claim 13 further comprising, if the way prediction is incorrect, replacing a cache line in the cache in the way indicated by the way prediction with a missing cache line corresponding to the first address.

22. (Original) The method as recited in claim 21 further comprising, if no way prediction is generated and a cache miss results for the first address, using a replacement algorithm to select the cache line to be replaced with the missing cache line.

23. (Currently Amended) An apparatus comprising:

a way predictor comprising:

a decoder configured to decode an indication of a first address that is to access a cache, the decoder configured to select a set responsive to the indication of the first address;

a memory coupled to the decoder, wherein the memory is configured to output a plurality of values from the set ~~a set of storage locations~~ in response to the decoder selecting the set, wherein each of the plurality of values corresponds to a different way of the cache, wherein each of the plurality of values comprises a plurality of bits

associated with a corresponding cache line in the cache; and

a first circuit coupled to receive the plurality of values and a first value corresponding to the first address, wherein the first circuit is configured to generate a way prediction for the cache responsive to the plurality of values and the first value; and

a data cache data memory coupled to the way predictor, wherein the data cache data memory is arranged into a plurality of ways, and wherein the data cache data memory is configured to output data from a predicted way of the plurality of ways, wherein the predicted way is identified by the way prediction, and wherein the data cache data memory includes a second circuit configured to reduce power consumption attributable to one or more non-predicted ways of the plurality of ways.

24. (Original) The apparatus as recited in claim 23 further comprising a data cache tag memory configured to output a tag from the predicted way and to not output tags from the one or more non-predicted ways.

25. (Original) The apparatus as recited in claim 23 wherein the second circuit is configured to generate separate wordlines for each of the plurality of ways in the data cache data memory, and wherein the second circuit is configured to activate a first wordline to the predicted way and to not activate word lines to the non-predicted ways responsive to the way prediction.

26. (Original) The apparatus as recited in claim 25 wherein the second circuit includes column multiplexor circuitry coupled to the plurality of ways and configured to select the output of the predicted way as input to a sense amplifier circuit, wherein the column multiplexor circuitry is controlled by the way prediction.

27. (Original) The apparatus as recited in claim 23 wherein the second circuit includes

column multiplexor circuitry coupled to the plurality of ways and configured to select the output of the predicted way as input to a sense amplifier circuit, wherein the column multiplexor circuitry is controlled by the way prediction.

28. (Original) The apparatus as recited in claim 23 wherein the second circuit comprises a plurality of sense amplifier circuits, wherein each of the plurality of sense amplifier circuits is coupled to a respective one of the plurality of ways, and wherein each of the plurality of sense amplifier circuits includes an enable input that is controlled by the way prediction.

29. (New) The apparatus as recited in claim 23 further comprising a second level cache, and wherein the circuit is configured to detect a miss responsive to the plurality of values and the first value prior to the miss being detected in the data cache that corresponds to the data cache data memory, and wherein the circuit is configured to signal the miss the second level cache, and wherein the second level cache is configured to begin an access corresponding to the first address responsive to signal from the circuit.